

ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device is provided to reduce the adverse effect of PWM noise occurring in a PWM driving section on an analog voltage processing section in an IC, in which digital and analog circuits are combined on a single chip. A sampling signal generation circuit outputs a sampling signal S_t to an A/D converter at a predetermined time when "delay time t_d + allowance time t_a " has elapsed from a start signal S_p . The delay time t_d is shorter than "the minimum time width of H level of PWM signal $SPWM1$ - allowance time t_a ". The delay time t_d is also time from the variation of level of the PWM signal $SPWM1$ to actual variation in the passage of current through a power section.